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10/696,146	10/29/2003	Michael B. Galles	062986.0296	5506

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EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
11/03/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/696,146	GALLES ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-10 and 16-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. The examiner is unable to find, in applicants' original disclosure, support for the claim language in claim 1 reciting "a central processing unit having an integrated memory controller operable to control access to the integrated memory nor support for the claim language in claim 16 reciting "a memory controller integrated in the central processing unit and operable to control access to and from local memory". There is nothing supporting the claim to the CPU having such a memory controller though there is support for the processor having such a controller. For this reason the examiner views the quoted language as representing new matter.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-10 and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. As to why the examiner cites claims 1-10 and 16-20 as failing to point out and distinctly claim applicants' invention, see paragraph 4, *supra*.

8. Applicants have argued that their Fig. 2 in conjunction with the language of page 7, lines 5-7 where it says "Each of the plurality of Processors 12 has a memory 16, a memory directory 18, and a central processing unit 20 all integrated into a single device", justifies the language cited in paragraph 5, *supra*. The only reasonable interpretation of the sentence recited at page 7, lines 5-7 is that the memory 16, the memory directory 18, and the central processing unit 20 are all part of a single device (i.e., the processor, as depicted in Figure 1). The language does not say "a central processing unit having an integrated memory controller operable to control access to the integrated memory" as claimed in claim 1 nor say "a memory controller integrated in the central processing unit and operable to control access to and from local memory" as claimed in claim 16. The language only says they are both part of the processor. Note, too, that the memory 16 is not even a part of Fig. 2. Therefore, it is hard to argue Fig. 2 depicts the single integrated device of page, 7, lines 5-7.

9. The examiner would reiterate applicants' original disclosure never offered a definition for integrated. And, while Fig. 1 shows a dotted line around relevant components labeled "processor" there is nothing in applicants' original disclosure to limit such components to the same computer chip or the same computer board, or same external housing, or same rack, or same room, etc. As shown in Figure 1 and as described in applicants' specification, applicants' system components do not seem to be integrated except in the sense they work with one another in terms of hardware and

software. If applicants are arguing something else for the claim language, this makes the subject matter of claims 1-10 and 16-20 new matter and also renders the scope of these claims indefinite. If they are not arguing anything more than they work with one another in terms of hardware and software, then the previous rejections of applicants' claims still apply.

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-2 and 4-20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kabemoto et al. (Patent No. 5,890,217).

12. The examiner would suggest applicants read col. 16, line 5 through col. 20, line 18 and col. 28, line 55 through col. 29, line 10, at a minimum, before responding.

13. The arguments and rejections presented in the examiner's previous rejections in parent application 09/418,520 and in this application continue and are hereby incorporated by reference.

14. Claims 1-2, 5-6, 9-11 and 13-17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chase et al. (Patent No. 5,944,780).

15. The examiner would suggest applicants read (col. 5, line 30 through col. 6, line 20; col. 7, lines 44-61; and col. 8, lines 42-48), at a minimum, before responding.

16. The arguments and rejections presented in the examiner's previous rejections in parent application 09/418,520 and in this application continue and are hereby incorporated by reference.

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19. Claims 3, 10, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chase et al. (Patent No. 5,944,780).

20. The arguments and rejections presented in the examiner's previous rejections in parent application 09/418,520 (in relation to claims 10, 18, and 20) and in this application continue and are hereby incorporated by reference.

21. As to claim 3, Chase taught the invention of independent claims 1 and 2 from which claim 3 depends (see paragraphs 6-8, *supra*). He did not teach overwriting the oldest memory reference with a new memory reference upon reaching a buffer limit nor any specific replacement strategy for such a situation. However, the examiner takes Official Notice of the fact that the least-recently-used method of replacement in caches is old, well-known, and one of the conventional methods of cache replacement. In fact, there are at least 267 patents making reference to it as a replacement strategy in subclass 711/133, alone, with the oldest one having been issued a quarter century ago. One of ordinary skill would be motivated to use the least-recently-used replacement strategy with Chase because it is a conventional method which is well-known and well-understood by those of ordinary skill and is, therefore, easily and reliably implemented.

22. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kabemoto et al. (Patent No. 5,890,217).

23. As to claim 3, Kabemoto taught the invention of independent claims 1 and 2 from which claim 3 depends (see paragraphs 6-8, *supra*). He did not teach overwriting the oldest memory reference with a new memory reference upon reaching a buffer limit nor any specific replacement strategy for such a situation. However, the examiner takes Official Notice of the fact that the least-recently-used method of replacement in caches is old, well-known, and one of the conventional methods of cache replacement. In fact, there are at least 267 patents making reference to it as a replacement strategy in subclass 711/133, alone, with the oldest one having been issued a quarter century ago. One of ordinary skill would be motivated to use the least-recently-used replacement

strategy with Chase because it is a conventional method which is well-known and well-understood by those of ordinary skill and is, therefore, easily and reliably implemented.

24. The examiner is unable to determine the true scope of applicants' claims 1-10 and 16-20, see paragraphs 2-9, *supra*, so the examiner has merely repeated his earlier rejection of those claims. As to amended claim 11, note that it is merely previously rejected claim 11 with much of the substance of previously rejected claim 13 incorporated therein. The only slight difference which might be perceived between current claim 11 and previously rejected claims 11 and 13 is the statement of the self-evident that when a memory reference is not found in the memory directory for the local memory then the reference is not to local memory but to a remote memory location. None of the amendments to claim 11 constitute patentable differentiation.

25. In reference to claim 11 and its dependents, applicants are repeating arguments the examiner dealt with exhaustively in parent application 09/418,520 so the examiner would refer them to that application. However, in response to applicants' argument that "Applicant's specification specifically shows that the term 'integrated' defines these elements as being within a single device, the processor", the examiner would reiterate applicants' original disclosure never offered a definition for integrated. And, while Fig. 1 shows a dotted line around relevant components labeled "'processor" there is nothing in applicants' original disclosure to limit such components to the same computer chip or the same computer board, or same external housing, or same rack, or same room, etc. The drawing provides no definition for the term integrated other than to say they work with one another in terms of hardware and software as do Chase's relevant components

(see parent application 09/418,520). As to applicants' arguments related to Kabemoto, the examiner would suggest applicants pay less attention to names and more attention to the teachings of Kabemoto. The processor element (14-1) of Figure 4 of Kabemote contains all the elements applicants are associating with their word, "processor", and Kabemoto even draws a line around his software and hardware integrated device while applicants only have a dotted line. Applicants are not trademarking a name. They are claiming an invention by claiming its elements. If the prior art has all of applicants' claim elements in a device the applicants choose to call a "duck" while the art calls it a "computer", applicants will still have no patentable differentiation.

26. The amendment filed 5/23/2006 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: The entire amendment to the specification on page 8 and on page 6 making Figure 2 a diagram of the central processing unit (20) when it was always described in the parent application (09/418,520) and its issued patent (6,651,157) as a diagram of a Processor 12.

27. Applicants are required to cancel the new matter in the reply to this Office Action.

28. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference signs) mentioned in the description: For Figure 2, many of the elements described as being elements of Figure 2 on pages 8 and 9 of the specification are, apparently, absent from the figure or mislabeled. Corrected drawing sheets in compliance with 37 CFR 1 .121(d) are required in reply to

the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

29. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference characters) not mentioned in the description: In Fig. 2 there is a box labeled 20 which is not described as an element of Fig. 2 in the detailed description of Figure 2 on pages 8 and 9 of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference characters) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

30. The examiner has objected to applicants' amendment to the specification as new matter and maintained his objection to the drawings. Applicants have offered no explanation as to why the description of Fig. 2 should be inconsistent with that of the parent application and its issued patent. Also, there is no satisfactory explanation as to why the error to be corrected is not merely changing the 20 to a 12 in Fig. 2.

31. Since applicants' arguments for their claims which were presented in the Supplemental Appeal Brief hinge on whether they have introduced new matter into their disclosure or not, the examiner has not responded to them except in his application of the following new grounds of rejection to meet the limitations introduced by the new matter.

32. For much of the recent prosecution history the examiner has been arguing with applicants over the introduction into the disclosure of what the examiner views as new matter. To make clear that applicants' claims, even with the new matter, are not patentable, the examiner is applying applicants' assignee's prior art to the claims in an obviousness rejection.

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

35. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laudon et al. ("The SGI Origin ...") in view of Yeager ("The MIPS R10000 ...") and Agarwal (An Evaluation of Directory Schemes for Cache Coherence).

36. Laudon substantially taught the invention of exemplary claim 1 including a multi-processor system (Fig. 1), comprising: a plurality of processors (Fig. 1, Proc A, Proc B, Node 1, ... Node 511), an external switch coupled to each of the plurality of processors (Hub Chip), the external switch operable to pass data to and from any of the plurality of processors (Fig. 2, Section 3.1 entitled Network Topology).

37. While the external switch/(Hub Chip) does not include "an external directory, the external directory operable to provide a memory reference for each of the plurality of processors to remote data that is not provided within its own integrated memory directory", Laudon taught the external directory (Fig. 1, Mem & Dir). It is not invention to take advantage of advances in the art (i.e., better fabrication technologies which permit more transistors and more features to be incorporated into a single device/chip thereby saving communication time and power once necessary to drive signals across chip boundaries) to integrate features into one chip which were once found in two or more computer chips. In other words, anyone of ordinary skill would know how to include the

Mem & Dir onto the Hub Chip based on advances in the fabrication art and would have motivation to do so based on the reduced time to propagate signals and the power savings.

38. Also, while Laudon did not specifically teach each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit having an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory, he did teach that his system can utilize two R10000 CPU chips with their external secondary caches in each node (Fig. 5, Section 3.3 entitled Node Design). And, Yeager makes clear each R10000 CPU chip has an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory (pp. 28-30). Note that Yeager depicts the same Hub Chip with Mem &Dir arrangement depicted in Laudon's Fig. 1 only Yeager identifies the Hub Chip as an External Agent, the Dir as a Directory, and the Mem as Duplicate Tags in his Fig. 1. Applicants mistakenly characterized the Directory of Fig 1 as the integrated memory directory of the R10000 processors. The examiner would suggest applicants read the section entitled Memory Hierarchy (pp. 37-39) where the TLB/(integrated memory directory) found in the R10000 is described. It is hard for the examiner to understand how applicants are so unfamiliar with the characteristics of their assignee's R10000 system even if they were somehow unfamiliar with a reference written by one of the designers of the R10000 system. Note

also that Yeager specifically taught that his system worked with directory based protocols as applicants' system does (System Flexibility, p. 29).

39. Finally, while it is unclear from Yeager what exact data is cached in the TLB/directory of his system (pp. 37-38, Memory Address Translation), it is clear that the values cached are for the most recently accessed memory references and that they can be compatible with a directory based system such as applicants' (System Flexibility, p. 29). Also, Agarwal (p. 353, Introduction, 3rd paragraph) makes clear that directory schemes such as applicants are describing in applicants' specification on p. 9, first paragraph, were known in the art 40 years ago.

40. In summary, all the elements of applicants' claim 1 were known in the art as well as how to connect such elements into directory based system such as applicants'. As quoted below from the MPEP where it discusses the KSR decision: When considering obviousness of a combination of known elements, the operative question is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." Applicants' improvement is not more than the predictable use of prior art elements according to their established functions.

41. Applicants response to the examiner's rejection seems to be predicated on the fact the examiner omitted reference to Agarwal in the form paragraph leading into the 103 rejection. The examiner is suggesting applicants review their response in light of Agarwal and some additional comments made by the examiner. Applicants have also argued the references separately as opposed to arguing the teachings of the combination as a whole.

42. As to claim 2, see the preceding paragraph.

43. As to claim 3, the examiner takes Official Notice of the fact that the least-recently-used method of replacement in caches is old, well-known, and one of the conventional methods of cache replacement. In fact, there are at least 267 patents making reference to it as a replacement strategy in subclass 711/133, alone, with the oldest one having been issued a quarter century ago. One of ordinary skill would be motivated to use the least-recently-used replacement strategy with the teachings of Laudon, Yeager, Agarwal because it is a conventional method which is well-known and well-understood by those of ordinary skill and is, therefore, easily and reliably implemented.

44. To assist applicants should they chose to challenge the examiner's Official Notice, the examiner is pointing out that following the KSR decision by the Supreme Court the Office has changed its policy related to Official Notice. The Office now requires applicants to provide persuasive evidence and/or arguments directly refuting the Official Notice before a supporting reference is to be supplied by the examiner.

45. As to claim 4, given the system for page migration taught by Laudon (Section 3.6, Performance Features) there would be times when the memory directory of a processor would hold references to data that had been requested and used but which was still in a page which had not been migrated from another node. Though unclear from applicants' claim language, this may also be a reference to a design choice which (by taking advantage of better fabrication technologies which permit more transistors and more features to be incorporated into a single device/chip) brings some of the

capabilities taught by Laudon for the external directory onto the CPU chip thereby permitting better integration of newer processor designs into the memory model.

46. As to claim 5-8, Laudon taught this as part of the cache coherence protocol (Section 3.6, cache coherence protocol, steps 1-2, 6a, and 6b of the basic flow for a read request).

47. As to claim 9, Laudon taught this (Section 3.3 entitled Node Design, "The system interface busses of the R10000 are connected to the Hub chip.").

48. As to claim 10, this is a reference to a design choice which (by taking advantage of better fabrication technologies which permit more transistors and more features to be incorporated into a single device/chip) brings capabilities taught by Laudon for the external directory onto the CPU chip thereby permitting better integration of newer processor designs into the memory model.

49. As to claims 11-17 and 19, they fail to teach or define over rejected claims 1-10.

50. Applicants have argued the steps of claim 11 somehow distinguish over the system of claim 1. In response the examiner would state applicants are merely claiming the steps inherent in the operation of a functioning version of the system of claim 1. If the system of applicants' claim 1 cannot perform the steps recited, it does not function as claimed in claim 1 and does not represent a useful invention.

51. As to claims 18 and 20, these are merely claims for size of a memory feature. Applicants have taught no new technology which results in a uniquely large size for their memory features. Absent such a teaching the size of the memory feature is merely a design choice readily implemented by one of ordinary skill.

52. MPEP 2141 reads, in part, as follows:

The Supreme Court in *KSR* reaffirmed the familiar framework for determining obviousness as set forth in *Graham v. John Deere Co.* (383 U.S. 1, 148 USPQ 459 (1966)), but stated that the Federal Circuit had erred by applying the teaching-suggestion-motivation (TSM) test in an overly rigid and formalistic way. *KSR*, 550 U.S. at, 82 USPQ2d at 1391. Specifically, the Supreme Court stated that the Federal Circuit had erred in four ways: (1) "by holding that courts and patent examiners should look only to the problem the patentee was trying to solve" (*Id.* at__ 82 USPQ2d at 1397); (2) by assuming "that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem" (*Id.*); (3) by concluding "that a patent claim cannot be proved obvious merely by showing that the combination of elements was obvious to try'" (*Id.*); and (4) by overemphasizing "the risk of courts and patent examiners falling prey to hindsight bias" and as a result applying "[r]igid preventative rules that deny factfinders recourse to common sense" (*Id.*).

In *KSR*, the Supreme Court particularly emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *Id*, at__82 USPQ2d at 1395, and discussed circumstances in which a patent might be determined to be obvious. Importantly, the Supreme Court reaffirmed principles based on its precedent that "the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. "*Id*, at__82 USPQ2d at 1395. The Supreme Court stated that there are "three cases decided after Graham [that] illustrate this doctrine." *Id*. at__82 USPQ2d at 1395. (1) "In *United States v. Adams*, ... [t]he Court recognized that when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result." *Id*. at__ 82 USPQ2d at 1395. (2) "in *Anderson's Black Rock, Inc. v. Pavement Salvage Co.*, ... [t]he two [pre-existing elements] in combination did no more than they would in separate, sequential operation" *Id*, at__82 USPQ2d at 1395. (3) "[I]n Sakraida v. A G Pro, Inc., the Court derived.., the conclusion that when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement the combination is obvious." *Id*. at, 82 USPQ2d at 1395-96 (Internal quotations omitted.). The principles underlining these cases are instructive when the question is whether a patent application claiming the combination of elements of prior art would have been obvious. The Supreme Court further stated that:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his ordinary skill. *Id*. at__82 USPQ2d at

> 1396. When considering obviousness of a combination of known elements, the operative question is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at__82 USPQ2d at 1396.

53. All the elements necessary to produce applicants' invention were well-known in the art. How one combined such elements to produce applicants' invention was also well-known in the art. One of ordinary skill would have readily recognized that the results of the combination were predictable. Absent some secondary considerations, not in evidence at this time, applicants' invention is obvious over the combination of prior art presented. The fact that applicants' drawings are merely block drawings, totally without any technical details as to how one of ordinary skill in the art might implement their invention, makes abundantly clear one of ordinary skill, at the time of their invention, knew how to create the components shown in the block drawings and how to integrate them as applicants' claim. Otherwise, applicants' system of claim 1 would not be enabled because there is a similar lack of any technical details for implementation in applicants' specification.

54. Applicant's arguments filed 7/24/2008 have been fully considered but they are not persuasive. See the preceding rejection of applicants' claims.

55. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

56. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/William M. Treat/
Primary Examiner, Art Unit 2181